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Transformerless Single-Phase Universal Active Filter with UPS Features and Reduced Number of Electronic Power Switches

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***Abstract*- This paper presents an universal active power filter for harmonic and reactive power compensation with UPS (Uninterrupted Power Supplies) features. The configurations does not use transformer in the series part. Transformerless modern UPS systems have been rapidly replacing the old technology due to their performance and size attributes. Reducing the numbers of passive elements and/or switches in active power filters and UPS topologies not only reduces the cost of the whole system but also provides some advantages, such as great compactness, smaller weight, and higher reliability. However, the cost reduction requires the use of more complex control strategies. The model of the proposed system is derived and it is observed that the system can be reconfigurable to operate with four or three-leg depending on the issue. A complete control system, including the PWM (Pulse-Width Modulation) techniques, is developed and a comparison between the proposed filter and the standard one is done, as well. Simulated and experimental results validate the theoretical considerations.**

***Keywords* – universal active power filter, single-phase structure, uninterrupted power supplies and PWM techniques.**

I. Introduction

The requirements of quality at power grids and increased sensitivity of the loads has stimulated the use of power electronics in context of power line conditioning [1]. Different equipments are used to improve the power quality, e.g., transient suppressors, line voltage regulators, uninterrupted power supplies, active filters, and hybrid filters [1], [2], [3], [4], [5], [6]. The continuous proliferation of electronic equipments either for home appliance or industrial use has the drawback of increasing the non-sinusoidal current into power grid. So, the need for economical power conditioners for single-phase systems is growing rapidly [2], [7], [8], [9], [10], [11]. Different solutions are currently proposed and used in practice applications to work out the problems of harmonics in electric grids. In the last decades, the use of active filtering techniques has became more attractive due to the technological progress in power electronic switching devices and more efficient control algorithms.

The issue of reducing the cost has been attracting the attentions of researchers. Generally, the largest cost reduction is achieved by reducing the number of switches employed in power converter or developing topologies that employ switches with lower voltage stresses. Cost reduction is also achieved by eliminating passive components such as inductors, capacitors and transformers. Reducing the numbers of switches and passive elements in Active Power Filters (APF) and Uninterrupted Power Supplies (UPS) topologies not only reduces the cost of the whole system but also provides some other advantages such as great compactness, smaller weight, and higher reliability [12], [13], [14], [15], [16], [17]. However, the cost reduction requires the use of more complex control strategies.

Uninterrupted power supplies are widely used to supply critical loads and provide reliable and high quality energy to the load [15], [18], [19], [20]. Static UPS systems are the most commonly used UPS systems. They have a broad variety of applications from low-power personal computer and telecommunication systems, to medium-power medical systems, and to high-power utility systems. The main advantages are high efficiency, high reliability, and low THD (Total Harmonic Distortion). The static UPS systems are classified into on-line, off-line and line-interactive.

This work will focus on the study of series-parallel line-interactive UPS topology, also known as delta converter, with reduced number of switches. The idea consists in developing a reconfigurable structure where one of the converter-leg can be used to charge the battery bank without having a dedicated d.c./d.c. converter, e.g., buck-boost converter. So, the configuration composed by four-leg converter can operates with three-leg leaving one leg to charge the battery bank. When the battery bank is charged, the system returns to its original form. A mathematical modelling and complete control system, including the PWM techniques, is presented. Simulated and experimental results validate the theoretical considerations.

II. Systems Modelling

The proposed configuration shown in Fig. 1 (a) comprise the grid (e_g, i_g), internal grid inductance (L_g), load Z_l (v_l, i_l),

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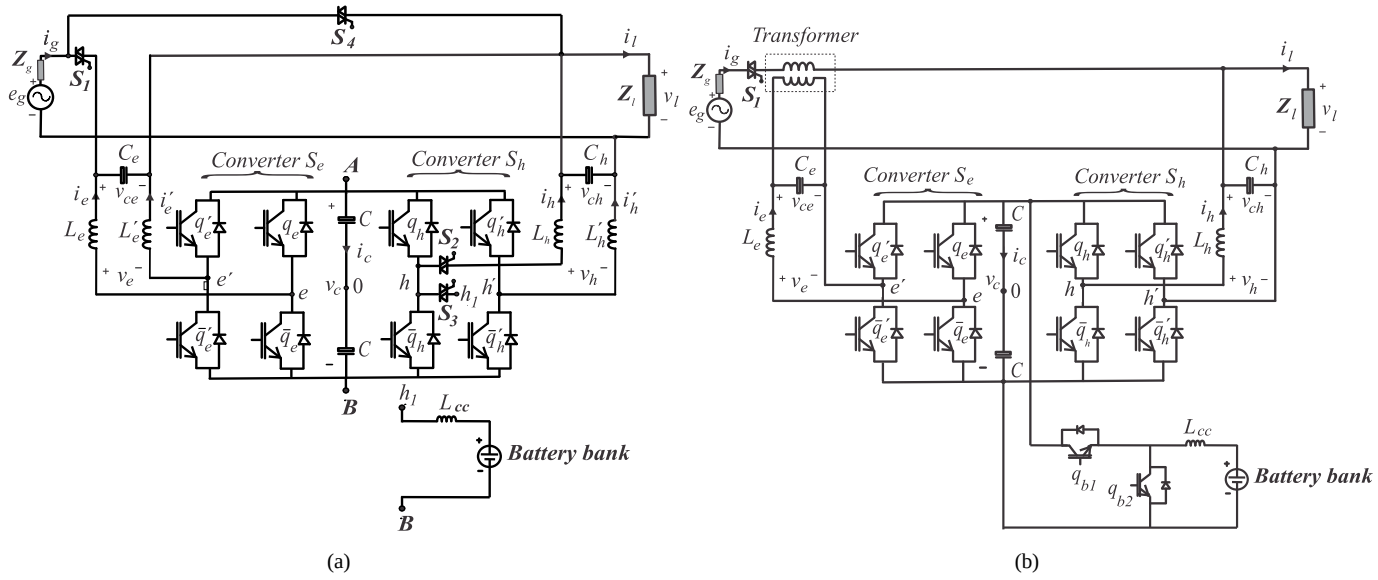

Fig. 1. Single-phase universal active filter topologies with UPS features. Proposed (a) and conventional (b).

converters S_e and S_h with a capacitor bank at the d.c.-link and filters Z_e (L_e, L'_e and C_e) and Z_h (L_h, L'_h and C_h). Converter S_e is composed by switches q_e, $\overline{q}_e$, q'_e and $\overline{q}'_e$. Converter S_h is composed by switches q_h, $\overline{q}_h$, q'_h and $\overline{q}'_h$. The conduction state of all switches is represented by an homonymous binary variable, where $q=1$ indicates a closed switch while $q=0$ an open one.

The difference between the two systems, Fig. 1, relates to components reduction. The proposed configurations, Fig. 1 (a), is transformerless and presents less power switches than the conventional, Fig. 1 (b). The idea of the proposed system is to utilize one of the converter-leg to charge the battery bank - when d.c. voltage level at the battery bank is beyond the preset tolerance - avoiding the necessity to have a dedicated d.c./d.c. buck-boost converter for it. The buck-boost converter of the conventional topology is composed by switches q_{b1} and q_{b2}. The filter inductance L_{cc} is common to both configurations. The system description with the power converter operating with four and three-leg is addressed.

A. Four-leg converter operation mode

The converter pole voltages v_{e0}, v'_{e0}, v_{h0} and v'_{h0} depend on the conduction states of the power switches, that is

$$v_{e0} = (2q_e - 1)\frac{v_c}{2} \tag{1}$$

$$v'_{e0} = (2q'_e - 1)\frac{v_c}{2} \tag{2}$$

$$v_{h0} = (2q_h - 1)\frac{v_c}{2} \tag{3}$$

$$v'_{h0} = (2q'_h - 1)\frac{v_c}{2} \tag{4}$$

where v_c is the d.c.-link voltage.

From Fig. 1(a), assuming that the switches S_1 and S_2 are on and S_3 and S_4 are off, the following equations can be derived considering the system operating with four-leg:

$$v_{e0} - v'_{e0} = v_g + \left[\frac{r'_e}{2} + \frac{r_e}{2} + \left(\frac{l_e}{2} + \frac{l'_e}{2}\right)p\right] i_e - v_l - \left(\frac{r'_e}{2} + \frac{l'_e}{2}p\right) i_o \tag{5}$$

$$v_{h0} - v'_{h0} = \left[\frac{r_h}{2} + \frac{r'_h}{2} + \left(\frac{l_h}{2} + \frac{l'_h}{2}\right)p\right] i_h + v_l + \left(\frac{r'_h}{2} + \frac{l'_h}{2}p\right) i_o \tag{6}$$

$$\begin{aligned} v'_{e0} - v'_{h0} = &-\left(\frac{r'_e}{2} + \frac{l'_e}{2}p\right) i_e + \left(\frac{r'_h}{2} + \frac{l'_h}{2}p\right) i_h + v_l \\ &+ \left[\left(\frac{r'_e}{2} + \frac{r'_h}{2}\right) + \left(\frac{l'_e}{2} + \frac{l'_h}{2}\right)p\right] i_o \end{aligned} \tag{7}$$

$$v_{e0} - v_{h0} = v_g - v_l + \left(\frac{r_e}{2} + \frac{l_e}{2}p\right) i_e - \left(\frac{r_h}{2} + \frac{l_h}{2}p\right) i_h \tag{8}$$

$$e_g - v_{ce} - v_l = (r_g + l_g p)\, i_g \tag{9}$$

$$pv_{ce} = \frac{1}{C_e}(i_g + i_e) \tag{10}$$

$$pv_l = \frac{1}{C_h}(i_g - i_l + i_h + i_o) \tag{11}$$

where $p = d/dt$, $v_g = e_g - r_g i_g - l_g p i_g$, $v_l = v_{ch}$ and i_l is calculated using the load model which can be linear or nonlinear; and symbols like r and l represent resistances and inductances of the inductors L_g, L_e, L'_e, L_h and L'_h. The circulating current i_o is defined by

$$i_o = i_e + i'_e = -(i_h + i'_h) \tag{12}$$

The resultant circulating voltage model is obtained by

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adding (5)-(8):

$$\begin{aligned} v_o = {} & v'_{e0} + v_{e0} - v'_{h0} - v_{h0} \\ & v_g + \left[\left(\frac{r'_e}{2} + \frac{r'_h}{2}\right) + \left(\frac{l'_e}{2} + \frac{l'_h}{2}\right)p\right] i_o \\ & + \left[\left(\frac{r_e}{2} - \frac{r'_e}{2}\right) + \left(\frac{l_e}{2} - \frac{l'_e}{2}\right)p\right] i_e \\ & - \left[\left(\frac{r_h}{2} - \frac{r'_h}{2}\right) + \left(\frac{l_h}{2} - \frac{l'_h}{2}\right)p\right] i_h \end{aligned} \tag{13}$$

The voltage v_o is used to compensate the circulating current i_o. The demonstration of this current can be seen in appendix of [16].

From the point of view of the controllers, the voltages: $v_e = v_{e0} - v'_{e0}$ (converter S_e) is used to regulate and compensate the load voltage v_l, $v_h = v_{h0} - v'_{h0}$ (converter S_h) regulates and controls the grid current in order to maintain the power factor close to one and $v_o = v'_{e0} + v_{e0} - v'_{h0} - v_{h0}$ (converter $S_e + S_h$) is used to cancel or gather the circulating current i_o near to zero.

In the balanced case, filter inductors are equal ($L_e = L'_e$ and $L_h = L'_h$) and the circulating voltage model become more simple, that is,

$$v_o = v_g + \left[\left(\frac{r_e}{2} + \frac{r_h}{2}\right) + \left(\frac{l_e}{2} + \frac{l_h}{2}\right)p\right] i_o \tag{14}$$

Thus, it can be noted that to minimize the circulating current i_o, the voltage v_o must be equal to v_g, i.e.

$$v_o = v_g \tag{15}$$

When $i_o = 0$ ($i_e = -i'_e$, $i_h = -i'_h$) the system model becomes:

$$v_{e0} - v'_{e0} = v_g + (r_e + l_e p) i_e - v_l \tag{16}$$

$$v_{h0} - v'_{h0} = (r_h + l_h p) i_h + v_l \tag{17}$$

$$e_g - v_{ce} - v_l = (r_g + l_g p) i_g \tag{18}$$

$$p v_{ce} = \frac{1}{C_e}(i_g + i_e) \tag{19}$$

$$p v_l = \frac{1}{C_h}(i_g - i_l + i_h) \tag{20}$$

This model is quite similar to the model of the conventional filter with an ideal transformer. Therefore, we can use $v_e = v_{e0} - v'_{e0}$ (converter S_e) to regulate the load voltage and $v_h = v_{h0} - v'_{h0}$ (converter S_h) to control the power factor and harmonics of i_g as in the conventional filter.

B. Three-leg converter operation mode

The system composed by three-leg works similar but, in this case, it has a shared-leg used by both converters (series and parallel filter) and a free-leg which is used to charge the battery bank when needed. The converter pole voltages v'_{e0}, v_{h0} and v'_{h0} depend on the conduction states of the power switches and may be expressed as

$$v'_{e0} = (2q'_e - 1)\frac{v_c}{2} \tag{21}$$

$$v_{e0} = (2q_e - 1)\frac{v_c}{2} \tag{22}$$

$$v'_{h0} = (2q'_h - 1)\frac{v_c}{2} \tag{23}$$

Assuming that the system operates with three-legs, considering the switches S_1 and S_3 are on and S_2 and S_4 are off, can write the following equations:

$$v_{e0} - v'_{e0} = v_g - v_l + \left(\frac{r_e}{2} + \frac{l_e}{2}p\right) i_e - \left(\frac{r'_e}{2} + \frac{l'_e}{2}p\right) i'_e \tag{24}$$

$$v'_{e0} - v'_{h0} = v_l + \left(\frac{r'_e}{2} + \frac{l'_e}{2}p\right) i'_e - \left(\frac{r'_h}{2} + \frac{l'_h}{2}p\right) i'_h \tag{25}$$

$$v_{e0} - v'_{h0} = v_g + \left(\frac{r_e}{2} + \frac{l_e}{2}p\right) i_e - \left(\frac{r'_h}{2} + \frac{l'_h}{2}p\right) i'_h \tag{26}$$

$$e_g - v_{ce} - v_l = (r_g + l_g p) i_g \tag{27}$$

$$p v_{ce} = \frac{1}{C_e}(i_g + i_e) \tag{28}$$

$$p v_l = \frac{1}{C_h}(i_g - i_l) \tag{29}$$

where $p = d/dt$, $v_g = e_g - r_g i_g - l_g p i_g$, $v_l = v_{ch}$ and i_l is calculated using the load model which can be linear or nonlinear. For this case, it is noted by the equations that there is no circulation current i_o.

III. PWM Strategy

This section presents the PWM Strategy for different modes of operations. Firstly, the system starts as four-leg converter and when is need to charge the bank of batteries it is reconfigurable to operate as three-leg. The descriptions of these modes of operations are presented as following.

A. Four-leg converter operation mode

Pulse-widths of gating signals can be directly calculated from the pole voltages $v^{*\prime}_{e0}$, v^*_{e0}, $v^{*\prime}_{h0}$ and v^*_{h0}.

Considering that v^*_e , v^*_h and v^*_o denote the reference voltages requested by the controllers (see Section IV), it comes

$$v^*_{e0} - v^{*\prime}_{e0} = v^*_e \tag{30}$$

$$v^*_{h0} - v^{*\prime}_{h0} = v^*_h \tag{31}$$

$$v^{*\prime}_{e0} + v^*_{e0} - v^{*\prime}_{h0} - v^*_{h0} = v^*_o. \tag{32}$$

Such equations are sufficient to determine the four pole voltages v^*_{e0}, $v^{*\prime}_{e0}$, v^*_{h0}, and $v^{*\prime}_{h0}$. Introducing an auxiliary variable v^*_x and choosing $v^{*\prime}_{e0} = v^*_x$, it can be written

$$v^*_{e0} = v^*_e + v^*_x \tag{33}$$

$$v^{*\prime}_{e0} = v^*_x \tag{34}$$

$$v^*_{h0} = \frac{v^*_e}{2} + \frac{v^*_h}{2} - \frac{v^*_o}{2} + v^*_x \tag{35}$$

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$$v_{h0}^{*\prime} = \frac{v_e^*}{2} - \frac{v_h^*}{2} - \frac{v_o^*}{2} + v_x^* \tag{36}$$

Two methods are presented in order to choose v_x^*.

Method A: General approach

In this approach, the reference voltage v_x^* is calculated by taking into account the maximum $v_c^*/2$ and minimum $-v_c^*/2$ value of the pole voltages, then:

$$v_{x\max}^* = v_c^*/2 - v_{\max}^* \tag{37}$$

$$v_{x\min}^* = -v_c^*/2 - v_{\min}^* \tag{38}$$

where v_c^* is the reference d.c.-link voltages, $v_{\max}^* = \max\vartheta$ and $v_{\min}^* = \min\vartheta$ with $\vartheta = \{v_e^*, 0, v_e^*/2 + v_h^*/2 - v_o^*/2, v_e^*/2 - v_h^*/2 - v_o^*/2\}$.

After v_x^* is selected, all pole voltages are obtained from (33)-(36). Then, v_x^* can be chosen equal to $v_{x\max}^*$, $v_{x\min}^*$ or $v_{x\text{ave}}^* = (v_{x\max}^* + v_{x\min}^*)/2$. Note that when $v_{x\max}^*$ or $v_{x\min}^*$ is selected, one of the converter-leg operates with zero switching frequency. On the other hand, operation with $v_{x\text{ave}}^*$ generates pulse voltage centered in the sampling period that can improve the THD of voltages.

The maximum and minimum values can be alternatively used. For example, during the time interval τ choose $v_x^* = v_{x\max}^*$ and in the next choose $v_x^* = v_{x\min}^*$. The interval τ can be made equal to the sampling period (the smallest value) or multiple of the sampling period to reduce the average switching frequency.

Once v_x^* is chosen, pole voltages $v_{e0}^{*\prime}$, v_{e0}^*, $v_{h0}^{*\prime}$ and v_{h0}^* are defined from (33)-(36). Since the pole voltages have been defined, pulse-widths τ_e, τ_e', τ_h and τ_h' can be calculated by:

$$\tau_e = \frac{T}{2} + \frac{T}{v_c} v_{e0}^* \tag{39}$$

$$\tau_e' = \frac{T}{2} + \frac{T}{v_c} v_{e0}^{*\prime} \tag{40}$$

$$\tau_h = \frac{T}{2} + \frac{T}{v_c} v_{h0}^* \tag{41}$$

$$\tau_h' = \frac{T}{2} + \frac{T}{v_c} v_{h0}^{*\prime} \tag{42}$$

Alternatively, the gating signals can be generated by comparing the pole voltage with a high frequency triangular carrier signal.

Method B: *Local approach*

In this case, the voltage v_{xs}^* is calculated by taking into account its maximum and minimum values in the series or shunt side. For example, if the series side is considered ($s = e$) then $v_{xe\max}^* = \max\vartheta_e$ and $v_{xe\min}^* = \min\vartheta_e$ with $\vartheta_e = \{v_e^*, 0\}$ and if the shunt side ($x = h$) is considered $v_{xh\max}^* = \max\vartheta_h$ and $v_{xh\min}^* = \min\vartheta_h$ with $\vartheta_h = \{v_e^*/2 + v_h^*/2 - v_o^*/2, v_e^*/2 - v_h^*/2 - v_o^*/2\}$. Besides these voltages, voltage v_x^* must also obey the other converter side**.** Then, these limits can be obtained directly from $v_{x\max}^*$ and $v_{x\min}^*$from (37) and (38).

The algorithm for this case is given by:

1) Choose the converter side to be the THD optimized and calculate v_{xs}^* between $v_{xs\max}^*$, $v_{xs\min}^*$ or $v_{xs\text{ave}}^* = (v_{xs\max}^* + v_{xs\min}^*)/2$.
2) Calculate the limits $v_{x\max}^*$ and $v_{x\min}^*$ from (37) and (38).
3) Do $v_{xs}^* = v_{x\max}^*$ if $v_{xs}^* > v_{x\max}^*$ and $v_{xs}^* = v_{x\min}^*$ if $v_{xs}^* < v_{x\min}^*$.
4) Do $v_x^* = v_{xs}^*$.
5) Determine the pole voltage and the gating signal as in previous method.

B. Three-leg converter operation mode

The pulse-widths of the gating signals can be directly calculated from the voltage referred to the d.c.-bus midpoint, which is given by the desired voltages for the grid and loads. If the desired phase voltages are specified as v_e^* e v_h^* then the reference midpoint voltages can be expressed as

$${v_{e0}'}^* = v_e^* + v_{e0}^* \tag{43}$$

$${v_{h0}'}^* = {v_h}^* + v_{e0}^* \tag{44}$$

Note that these equations cannot be solved unless v_{e0}^* is specified. Relations (43) and (44) can be formulated as

$${v_{e0}'}^* = v_e^* + v_\mu^* \tag{45}$$

$${v_{h0}'}^* = {v_h}^* + v_\mu^* \tag{46}$$

$$v_{e0}^* = v_\mu^* \tag{47}$$

The problem to be solved is to determine ${v_{e0}'}^*$, ${v_{h0}'}^*$ and v_{e0}^* from (45) - (47), once the desired voltage v_e^* and v_h^* have been specified. In the following, two techniques will be presented for generating the PWM gating signals for the converters.

Method A: General approach

The voltage v_μ^* can be calculated taking into account the general apportioning factor μ, that is

$$v_\mu^* = E\left(\mu - \frac{1}{2}\right) - \mu v_{\max}^* + (\mu - 1) v_{\min}^* \tag{48}$$

where: $v_{\max}^* = \max(v_e^*, v_h^*, 0)$ and $v_{\min}^* = \min(v_e^*, v_h^*, 0)$.

The apportioning factor μ $(0 \le \mu \le 1)$ is given by

$$\mu = \frac{t_{oi}}{t_o} \tag{49}$$

and indicates the distribution of the general free-wheeling period t_o (period in which voltages v_{e0}', v_{h0} and v_{e0} are equals) between the beginning $(t_{oi} = \mu t_o)$ and the end $(t_{of} = (1-\mu)\, t_o)$ of the switching period. The apportioning factor can be changed as a function of the modulation index (μ) to reduce the THD of both converter voltages.

In this case, the proposed algorithm is:

1) Choose the general apportioning factor μ and calculate v_μ^* from (48).
2) Determine ${v_{e0}'}^*$, ${v_{h0}'}^*$ and v_{e0}^* from (45) - (47).
3) Finally, once the midpoint voltage have been determined, calculate pulse-widths τ_e, τ_e' and τ_h'.

$$\tau_e = \frac{T}{2} + \frac{T}{E} v_{e0}^* \tag{50}$$

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$$\tau_e' = \frac{T}{2} + \frac{T}{E} {v'_{e0}}^* \tag{51}$$

$$\tau_h' = \frac{T}{2} + \frac{T}{E} {v'_{h0}}^* \tag{52}$$

Method B: *Local approach*

The voltage v_μ^* can be calculated taking into account the local apportioning factor μ_s:

1) for the grid $\mu_s = \mu_e$, dividing (splitting) the period t_{oe}, in which the voltages v'_{e0} and v_{e0} are equal, at the beginning ($t_{oie} = \mu_e t_{oe}$) and at the end ($t_{ofe} = (1-\mu_e)\, t_{oe}$) of the switching period.
2) for the load $\mu_s = \mu_h$, splitting the period t_{oh}, in which the voltages v'_{h0} and v_{e0} are equal, at the beginning ($t_{oih} = \mu_h t_{oh}$) and at the end ($t_{ofh} = (1-\mu_h)\, t_{oh}$) of the switching period.

Thus, the reference voltage $v_{\mu s}^*$ can be expressed by:

$$v_{\mu s}^* = E\left(\mu_s - \frac{1}{2}\right) - \mu_s v_{s\max}^* + (\mu_s - 1)\, v_{s\min}^* \tag{53}$$

where $v_{s\max}^* = \max V_e$ and $v_{s\min}^* = \min V_g$ if $s = e$ or $v_{s\max}^* = \max V_h$ and $v_{s\min}^* = \min V_h$ if $s = h$, where $V_e = \{v_e^*, 0\}$ and $V_h = \{v_h^*, 0\}$. Besides (53), the voltage $v_{\mu s}^*$ must also obey the other converter side. Then, from (45) and (46) the limits for $v_{\mu s}^*$ can be calculated

for $s = e$:

$$v_{\mu s\,\max}^* = \frac{E}{2} - v_h^* \tag{54}$$

$$v_{\mu s\,\min}^* = -\frac{E}{2} - v_h^* \tag{55}$$

for $s = h$:

$$v_{\mu s\,\max}^* = \frac{E}{2} - v_e^* \tag{56}$$

$$v_{\mu s\,\min}^* = -\frac{E}{2} - v_e^* \tag{57}$$

In this case, it is possible to control how the harmonic distortion is divided by both converters. So, the proposed algorithm is:

1) Choose the local apportioning factor μ_s so that grid or load converter is optimized, calculate $v_{\mu s}^*$ from (48).
2) Determine ${v'_{e0}}^*$, ${v'_{h0}}^*$ and v_{e0}^* from (45) - (47) using $v_\mu^* = v_{\mu s}^*$.
3) Use Step 3 of Method A.

IV. Overall Control Strategy

As mentioned in the previous sections, the modes of operation of the converter is defined by the system functionality. The system can operate with four or three-leg depend on the need; or in case of grid voltage fault, the battery bank is used to supply energy to the d.c.-bus capacitor voltage and inverter in order to maintain the desirable voltage to the load.

The description of the operation mode of the proposed circuit can be observed at Fig. 2. The image in gray represents the section of the circuit that is not in use. Four operation modes are presented. In Fig. 2(a), the system operates with four-leg. In three-leg mode, presented at Fig 2(b), the free-leg denoted by *h* is not in use. At Fig. 2(c), the system is still operating in three-leg mode and the free-leg is used to charge the battery bank, operating as buck converter. Finally, assuming the battery charged, the Fig. 2(d) presents the condition in which the energy is transferred from the battery bank to the load via inverter, considering the failure at the a.c. input. At this mode, the leg *h* works as boost converter.

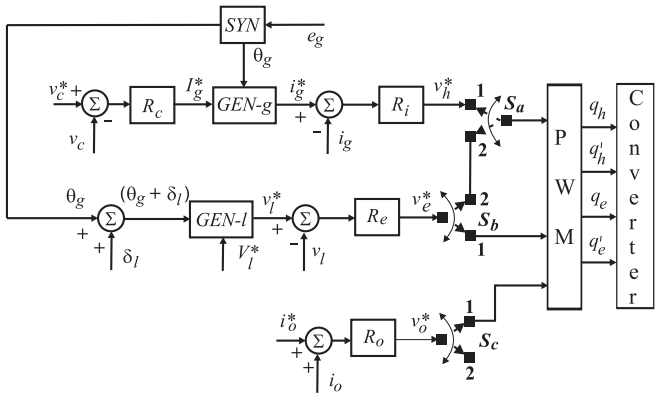

Fig. 3. Control block diagram of the proposed configuration.

The proposed system control is shown in 3. The mode of operation of the converter is determined by the state of switch S_c. If S_c is in position 1, the converter operates according to the four-leg mode. If S_c is in position 2, the selected mode is three-leg. The disconnection of the circulating current control block makes possible to use the shared-leg to charge the battery bank.

For the system operating with four-leg, switches S_a, S_b and S_c in position 1, the capacitor d.c.-link voltage v_c ($v_c = E$) is adjusted to a reference value by using the controller R_c, which is a standard PI type controller. This controller provides the amplitude of the reference current I_g^*. For the power factor and harmonic control the instantaneous reference current i_g^* must be synchronized with voltage e_g. This is performed by the block GEN-g, from a PLL scheme. From the synchronization with e_g and the amplitude I_g^*, the current i_g^* is generated. The current controller is implemented by using the controller indicated by block R_i. The controller R_i is a double sequence digital current controller employed in [21]. Thus current controller defines the input reference voltage v_h^*.

The instantaneous reference load voltage v_l^* can be determined by using the rated optimized load angle δ_l plus the information θ_g from block SYN and the defined load amplitude V_l^*. The block GEN-l uses the input information to generate the desired reference load voltage v_l^*. The homopolar current i_o is controlled by controller R_o, that determines voltage v_o^* responsible to minimize the effect of the circulating current i_o, maintaining this current near to zero. All these voltages are applied to PWM block to determine the conduction states of the converter's switches.

When the switch S_c is in position 2, three-leg mode of operation occurs. The d.c./d.c. buck converter is used to charge the battery bank. The free-leg makes the d.c.-bus voltage V_{cc} to be stepped down in its average value to supply the d.c.-battery

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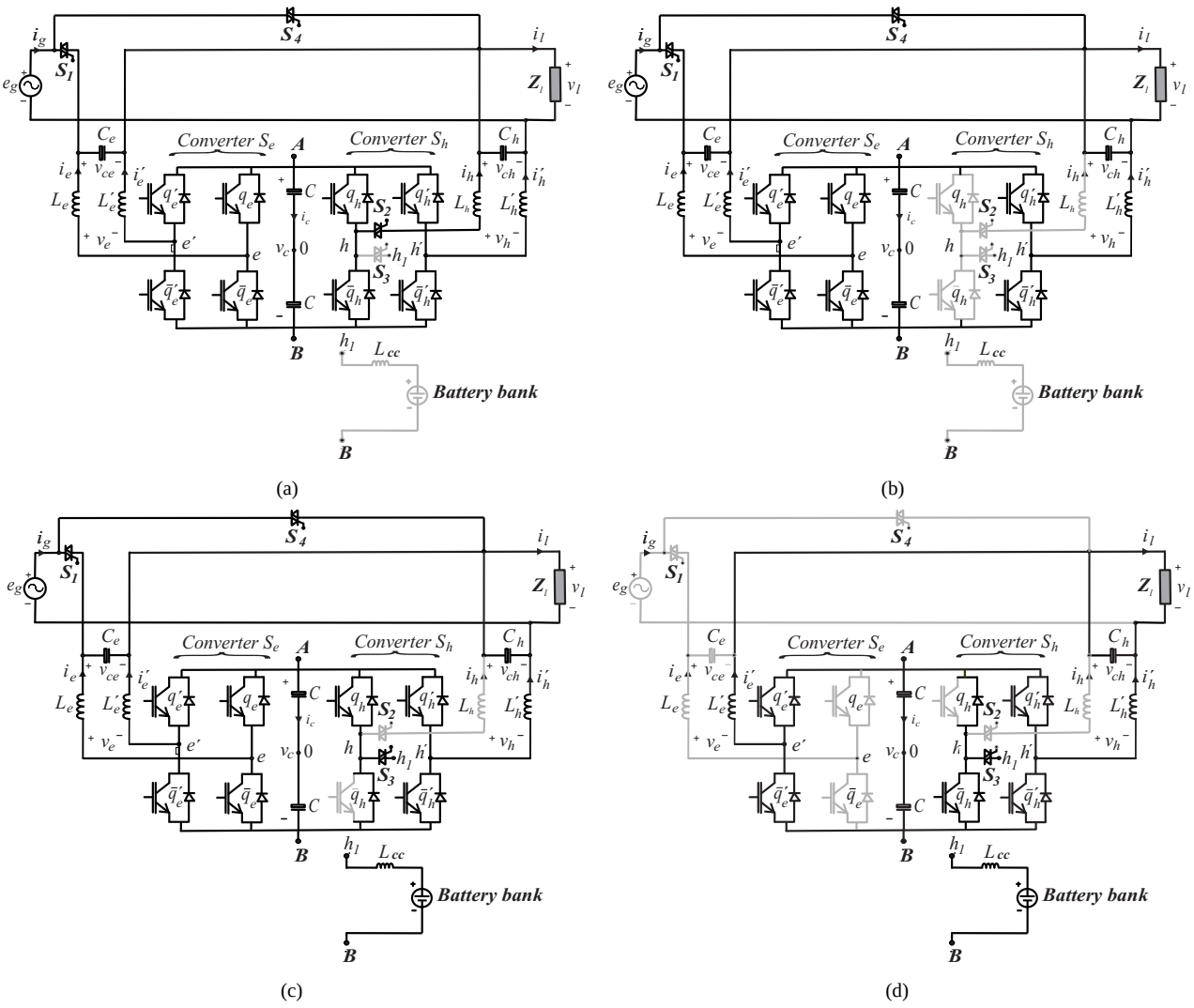

Fig. 2. Description of modes of operations: a) Four-leg mode; b)Three-leg mode; c) Three-leg mode charging the battery bank; d) Failure at the a.c. input.

bank according to $V_{bat} = DV_{cc}$. The battery voltage V_{bat} is directly proportional to duty ratio D. In the stored-energy mode of operation, when the a.c. input voltage is beyond the permissible tolerance range, the switch S_1 disconnects the a.c. input, transferring the energy from the battery bank to the load via inverter. Since the battery voltage is low, it is first requires to be boosted to high d.c. voltage for the proper operation of the d.c./a.c. inverter, now responsible to supply the load. The low battery voltage V_{bat} is boosted to high d.c. voltage V_{cc} according to $V_{cc} = V_{bat}/(1 - D)$.

When both switches S_a and S_b are in position 2, situation in what the a.c. input voltage failure, the load is supplied by battery bank and inverter. At this point, the converter S_h who was responsible for regulating the grid current and the d.c.-bus voltage is now responsible for maintaining the voltage applied to the load.

V. Simulation Results

The proposed configuration was simulated using PSIM software with the following parameters described in TABLE I. This configurations does not use transformer in the series connection and consist of four-leg converter. The converter can be reconfigured to work with three-leg in order to use the free-leg to charge the battery bank when needed. The free-leg is used to compose the buck converter controlling the duty ratio of the upper switch while the lower is idle. Some simulation results are now presented in Figs. 4, 5, 6 and 7. In the simulation results, the capacitors were selected

TABLE I

Parameters of the simulated system.

Parameter	Value
DC-bus voltage	$300V$
Battery bank voltage	$48V$
Inductance filter	$5.0mH$
Capacitor filter	$70uF$
Grid - voltage/frequency (e_g)	$110V/60Hz$
Harmonic component - amplitude/frequency	$0.2e_g/180Hz$
Load voltage (v_l)	$110V$
Power	$1.2kVA$
RL load	15Ω/2.0mH
Diode bridge rectifier connected to RLC	15Ω/2.0mH/2.0mF

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as $C = 2200\mu F$ and the switching frequency employed was $15kHz$. In each figures, there are four subfigures that describe

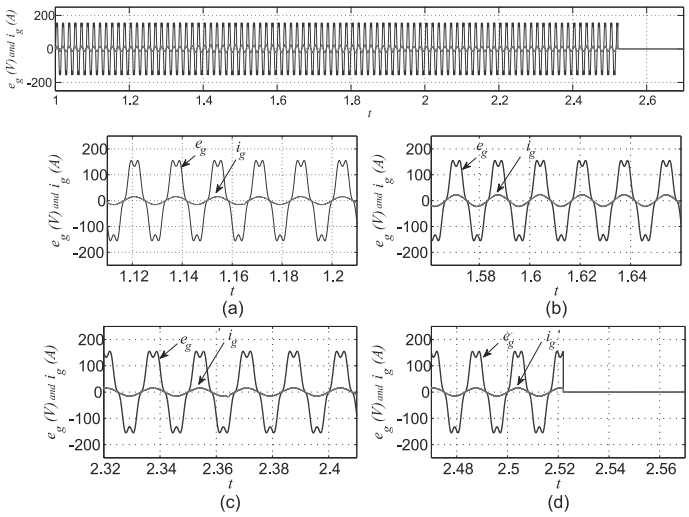

Fig. 4. Simulation results of the proposed system: grid voltage (e_g) and grid current (i_g).

the behavior of the system at certain intervals described as: (a) converter mode of operation of four-leg to three-leg (both switches S_2 and S_3 will be open) - the shared-leg is denoted by e and the free-leg is h, (b) storing-mode of operation (switch S_3 will be close), (c) converter mode of operation of three-leg to four-leg (both switches S_2 and S_3 will be close) and (d) the fault at a.c. input grid voltage with its disconnction from switch S_1. In Fig 4 is presented the grid voltage, with a disturbance of 20% of third harmonic, and current with power factor control near to unity. The THD of grid current is 3.91% and the load current and voltage THD are equal to 31,02% and 2,54%. During the storing-mode of operation, when the d.c. voltage level at the battery bank is beyond the preset tolerance, it is observed a certain increase at the grid current amplitude i_g, it happens because at this mode of operation the system needs to drain more current to maintain the voltage at d.c.-bus capacitors and to charge the d.c.-battery bank (Figs. 4 and 5). During this stage, the grid current THD increases a little to 4.36%. The load and grid voltages are also shown in Fig 6. In all subfigures labeled as (d) are described the moment when the fault at a.c. grid voltage occurs and the load is supplied by boost converter via free-leg and inverter maintaining the load voltage at desired value.

The d.c.-bus voltage is shown in Fig. 7. At time t_1, it is depicted converter mode of operation of four to three-leg. During t_2 - t_3, it observed the interval the battery bank is being charged. The change in the mode of operating of three-leg to four-leg occurs at t_4. The battery charging voltage is 48 V_{cc} as observed in Fig. 7 (b). The presented result illustrates only the interval the battery bank is being charged taking as reference the coupling point connection *hB*, see Fig. 1(a). Finally, at t_5, where the a.c. grid voltage failure, it is show the instant the system is supplied by battery bank and inverter which keeps the voltage to the load at the desired value.

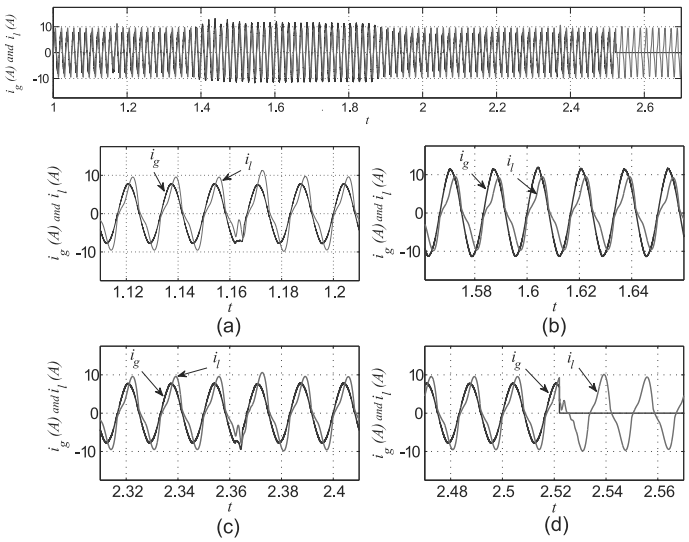

Fig. 5. Simulation results of the proposed system: grid current (i_g) and load current (i_l).

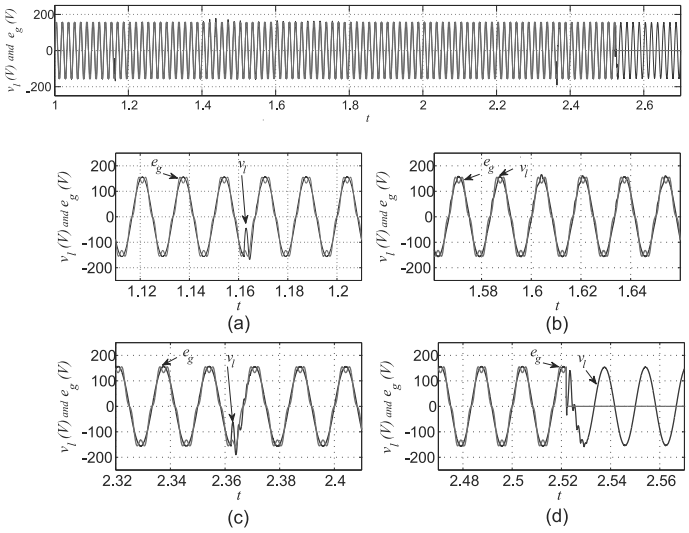

Fig. 6. Simulation results of the proposed system: grid voltage (e_g) and load voltage (v_l).

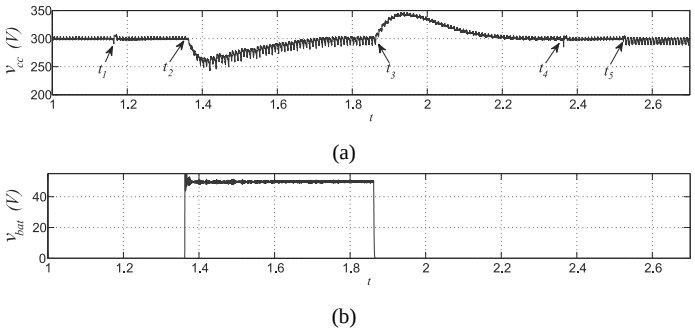

Fig. 7. Simulation results of the proposed system: a) d.c.-bus voltage. b) battery-bank voltage - storing-mode of operation (from the coupling point *hB*).

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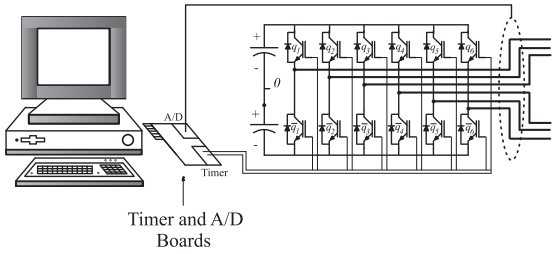
TABLE II

PARAMETERS OF THE TEST BENCH.

Parameter	Value
DC-bus voltage	$250V$
Battery bank voltage	$48V$
Inductance filter	$7.0mH$
Capacitor filter	$70uF$
Grid - voltage/frequency (e_g)	$110V/60Hz$
Harmonic component - amplitude/frequency	$0.2e_g/180Hz$
Load voltage (v_l)	$110V$
Power	$1.2kVA$
RL load	15Ω/2.0mH
Diode bridge rectifier connected to RLC	15Ω/2.0mH/2.0mF

VI. EXPERIMENTAL RESULTS

In this section, experimental results of the proposed system are presented. The system operates at four-legs mode which is reconfigurable to operate with three-legs in order to charge the battery bank performing voltage and current compensation. The proposed topology, Fig. 1(a), has been tested by using a microcomputer-based system which is equipped with dedicated boards, in order to generate the control signals. The system have twelve sensors (six current and six voltage sensors), interface card and data acquisition boards, and two static converters each one with three-leg, see Fig. 8. In the



(a)

(b)

Fig. 8. Experimental platform in laboratory:(a) Schematic diagram of the converter via PC-based control, (b) Picture of the topology.

experimental tests, the capacitors were selected as $C = 2200\mu F$ and the switching frequency employed was $15kHz$. The system parameters are presented in TABLE II.

In Fig. 9 are shown the grid current (i_g), the grid voltage (e_g), the load current (i_l) and the load voltage (v_l). The grid voltage has been obtained from a disturbance voltage source and even in the presence of 20% of third harmonic voltage

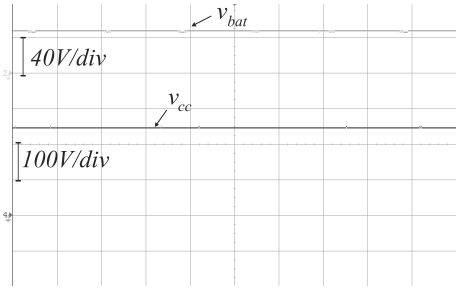


Fig. 9. Experimental results of the proposed system: grid voltage (e_g) and grid current (i_g) [top]; load voltage (v_l) and load current (i_l) [bottom]. Vertical: 100 V/div and 5A/div.

at grid; the grid current and the load voltage present the waveform characteristic close to sinusoidal and with power factor control close to one. The grid current THD is 4.36%, while the load current presents THD equal to 29.94%. The load voltage THD, for this case, is equal to 2.98%. The voltage

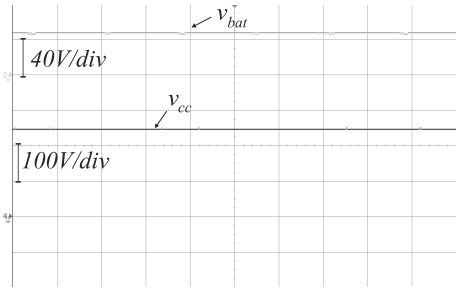


Fig. 10. Experimental results of the proposed system: battery bank voltage (v_{bat}) and d.c.-bus voltage (v_{cc}). Horizontal: 5ms/div.

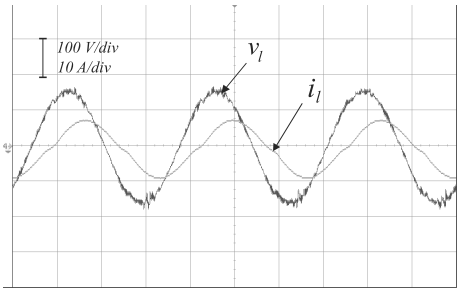


Fig. 11. Experimental results of the proposed system: load voltage (v_l) and load current (i_l). Vertical: 100 V/div and 5A/div.

of both d.c.-bus voltage and battery bank during the storing - mode of operation are indicated in Fig. 10. For the d.c.-bus voltage and battery bank control it was chosen $250V_{cc}$ and $48V_{cc}$, respectively. After the fault at a.c. grid voltage the inverter via boost converter keeps the desired voltage to the load, as shown in Fig. 11.

VII. CONCLUSIONS

An universal active power filter for harmonic and reactive power compensation with UPS features for single-phase system has been presented. The proposed configuration is a transformerless delta converter with reduced number of components that that emulates the buck-boost converter from

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the shared-leg. The system modelling of the proposed system shows that the circulating current can be controlled to a level near to zero. The control of the circulating current is accomplished by the voltage $v_o = v'_{e0} + v_{e0} - v'_{h0} - v_{h0}$ (converters $S_e + S_h$) in order to control the i_o close to zero. In the three-legs mode of operation, the circulating current does not exist. A suitable control strategy for the proposed system, including PWM techniques has also been presented. The system can be reconfigurable to operate with four or three-leg leaving the free-leg to charge the battery bank without having a dedicated d.c./d.c. buck-boost converter. The configuration produces satisfactory results. The proposed solution has the advantage of reducing volume and cost in comparison to the conventional UAPF. Simulated and experimental results have been presented and validates the operation of the proposed system.

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